

Application No. 10/826,039
Response to Office Action

Customer No. 01933

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:
a semiconductor construction assembly ~~having~~ including:

~~(i) a semiconductor substrate which has one surface, the other~~
~~surface facing said one surface, having first and second surfaces~~
5 ~~that are mutually opposed to each other, and a plurality of side~~
~~surfaces between said one the first surface and the other second~~
~~surface, and has~~ (ii) an integrated circuit element formed on
~~said one the first surface, (iii) a plurality of connection pads~~
~~which are arranged on said one the first surface and connected to~~
10 ~~the integrated circuit element, (iv) a protective layer which is~~
~~formed to cover said one the first surface of the semiconductor~~
~~substrate and which has openings for exposing the connection~~
~~pads, and (v) a plurality of conductors which are connected to~~
~~the connection pads [[,]] and arranged on the protective layer~~
15 ~~[[,]] and which have pads, (vi) columnar electrodes formed on the~~
~~pads of the conductors, and (vii) a sealing film formed between~~
~~the columnar electrodes and on the protective layer;~~

~~an upper insulating layer which entirely covers said one~~
~~surface of the semiconductor construction assembly including the~~
20 ~~conductors except the pads,~~

a sealing member which covers at least one side surface of
the semiconductor construction assembly; and

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25 an upper insulating layer which covers the semiconductor
 construction assembly and the sealing member except for portions
 corresponding to the columnar electrodes so as to expose an upper
 surface of each of the columnar electrodes;

30 upper conductors which are formed on the upper insulating
 layer, and ~~has~~ each of which includes one ends end that is
 electrically connected to the ~~pads~~ pad of one of the conductors
 via one of the columnar electrodes and an at least one external
 connection pads, respectively, pad;

wherein an external connection pad of at least one of the
 upper conductors ~~being~~ is disposed in a region ~~corresponding to~~
 opposing the sealing member.

Claim 2 (Canceled).

3. (Currently Amended) A semiconductor device according to
claim 1, wherein an additional insulating layer made of an
inorganic material is formed between the semiconductor substrate
and the protective layer of the semiconductor construction
assembly.

4. (Currently Amended) A semiconductor device according to
claim 1, wherein upper surfaces of the sealing member and the
semiconductor construction assembly are substantially flush with
each other.

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5. (Currently Amended) A semiconductor device according to claim 1, wherein lower surfaces of the sealing member and the semiconductor construction assembly are substantially flush with each other.

Claims 6 and 7 (Canceled).

8. (Original) A semiconductor device according to claim 1, further comprising a base member which holds the semiconductor construction assembly and the sealing member.

9. (Original) A semiconductor device according to claim 8, wherein the base member is made of a heat dissipation material.

10. (Original) A semiconductor device according to claim 8, further comprising an insulating layer which fixes the semiconductor construction assembly to the base member.

11. (Currently Amended) A semiconductor device according to claim 1, wherein the sealing member ~~includes~~ comprises a buried member.

12. (Currently Amended) A semiconductor device according to claim 11, wherein the buried member has substantially ~~the~~ a same thickness as a thickness of the semiconductor construction assembly.

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13. (Currently Amended) A semiconductor device according to claim 11, wherein ~~an~~ a further insulating material is filled between the buried member and the semiconductor construction assembly.

14. (Original) A semiconductor device according to claim 1, wherein interlayer conductors which connect the conductors of the semiconductor construction assembly and the upper conductors, and an interlayer dielectric layer which covers the interlayer
5 conductors are arranged between the upper conductors and the semiconductor construction assembly.

15. (Currently Amended) A semiconductor device according to claim ~~±~~ 14, wherein an uppermost insulating layer is arranged on an upper surface of the interlayer dielectric layer ~~including and on~~ the upper conductors ~~except and does not cover~~ the external connection pads of the upper conductors.

16. (Currently Amended) A semiconductor device according to claim 15, wherein further comprising projecting connection terminals ~~are~~ arranged on the external connection pads of the upper conductors.

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17. (Currently Amended) A semiconductor device according to claim 16, wherein each of the projecting connection terminals ~~includes~~ comprises a solder ball.

18. (Withdrawn - Currently Amended) A semiconductor device according to claim 15, wherein ~~an~~ at least one electronic component which is electrically connected to at least one of the external connection pads is arranged on the uppermost insulating layer.

19. (Withdrawn - Currently Amended) A semiconductor device according to claim 15, wherein ~~a~~ at least one connection pin is arranged on at least one of the external connection pads.

20. (Withdrawn - Currently Amended) A semiconductor device according to claim 1, further comprising ~~an~~ at least one electrical connection member which is electrically connected to at least one of the upper conductors, and ~~extend~~ which extends vertically through the sealing member ~~to the other~~ from an upper surface of the sealing member to a lower surface of the sealing member.

Claim 21 (Canceled).

22. (Currently Amended) A semiconductor device comprising:
a semiconductor construction assembly ~~having~~ including
projecting electrodes which are coupled to pads of a semi-

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conductor substrate and which have substantially flat respective
5 upper surfaces, and a sealing member which is formed between the
projecting electrodes and covers one an upper surface of a the
semiconductor substrate while externally exposing at least ~~on the~~ the
upper ~~surface~~ surfaces of ~~a the~~ the projecting ~~electrode~~ electrodes
such that the substantially flat upper surfaces of the projecting
10 electrodes and an upper surface of the sealing member are
substantially flush with each other;

an upper insulating layer which covers one entire surface of
the semiconductor construction assembly;

a second sealing member which covers a side surface of the
15 semiconductor construction assembly; and

an upper conductor which is formed on the upper insulating
layer, is electrically connected to the projecting electrode, and
extends to a region corresponding to the second sealing member.

23. (Currently Amended) A semiconductor device comprising:

a plurality of semiconductor construction assemblies
separately arranged from each other, each having including
projecting electrodes which are coupled to pads of a
5 semiconductor substrate and which have flat respective upper
surfaces, and an organic insulating film which is formed between
the projecting electrodes and covers one an upper surface of a
the semiconductor substrate while externally exposing at least ~~an~~

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